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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,230	12/02/2003	Serge Francois Drogi	55123P265	5369

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EXAMINER	
VLAHOS, SOPHIA	
ART UNIT	PAPER NUMBER
2611	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/727,230	DROGI ET AL.	
	Examiner	Art Unit	
	SOPHIA VLAHOS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-94* is/are pending in the application.

4a) Of the above claim(s) *1-85* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *86-94* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/27/08, 4/18/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments, see Remarks, filed 4/23/08, with respect to the rejection(s) of claim(s) 86, 91,94 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Maligeorgos et al. (U.S. 7,221,921) and Koch et al. WO 03/050941 (published on 6/19/03).

Applicant argues: "Fig. 9 clearly shows serial clock signals SCLK as well as serial data SDI into and out of block 905. Clearly the examiner is wrong on this point. "

With respect to the signals into and out of block 905, the above description is accurate. However in the art rejection of claim 86, block 910 "Receiver Analog Circ." corresponds to the first integrated circuit, blocks 905, 120 correspond to the second integrated circuit. Received data flows from block 910 to blocks 905&120. Therefore the first integrated circuit (910) **does not output a clock signal** to blocks 905&120 (although it receives a clock signal 950 from the second integrated circuit).

Nevertheless, the newly found reference that teaches external clocking, instead of clock transfer among integrated circuits is relied upon for art rejections.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 90, 93, 94 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 90 recites: "… and the first integrated circuit is configured to… recover the digital data to be transmitted and modulate the digital data for RF transmission." The pertinent paragraphs in the printed application publication U.S. 2005/0118977 are ¶0077-0082 relating to Fig. 3C, and there is no modulation of digital data for RF transmission performed by the first integrated circuit.

Claims 93 and 94 recite similar limitations and are also rejected based on the same rationale.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary

skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 86-88, 89 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maligeorgos et al., (U.S. 7,221,921) in view of Koch et al. WO 03/050941 (published on 6/19/03).

With respect to claim 86, Maligeorgos et. al., disclose: a first integrated circuit for receiving an RF signal and converting the RF signal to a baseband signal (Fig. 2D , Rx analog circuitry 208, more details shown in Fig. 8, block 839, where the outputs of the down-converter 409, are baseband signals (I and Q), see column 10, lines 46-48, column 19, lines 5-10) and for converting the baseband signal to a serial digital signal using a one-bit sigma delta modulator (block 836, ADC circuit, column 19, lines 20-25, column 21, lines 48-51 sigma-delta ADC) for output to a second integrated circuit (Fig. 2D the Rx Digital circuit is part of the baseband processor and/or Fig. 8 see transmission of serial digital baseband signals from Rx Analog circuit to Rx Digital circuit (Fig. 9A see blocks 910 (Rx Analog circuit) and 905 & 120(Rx Digital circuit and baseband circuit) lines 960, 965 used for received data transmission to Rx Digital circuit) and the second integrated circuit having a digital signal processor for receiving the serial digital signal output of the first integrated circuit (embodiment shown in Fig. 2D, and column 16, lines 23-26 where the functionalities of the Rx Digital circuit are assumed by the baseband processor (DSP see column 9, lines 35-39)), and recovering digital data in the received RF signal (see Fig. 11A, Rx digital side, the recovered digital data correspond to the realigned digital I and Q signals out of 1123A and 1123B that are supplied to other circuits in the baseband

processor, and since the invention relates to cellular applications (see column 2, lines 56-58) it is understood that voice signals (as an example) are output from the reconstructed digital signals)

Maligeorgos et al., do not expressly teach: without a data rate clock; reconstructing the data rate clock.

Solving the problem of clock transfer between circuits, Koch et al. disclose: without a data rate clock; reconstructing the data rate clock (Fig. 2 and Fig. 4 embodiments, see clock signal is not transferred (output) between the two integrated circuits (as in Fig.1) but supplied from an external source, Fig. 4, blocks "clock processing" include clock reconstruction, see page 2, lines 21-28, page 3, lines 31-35, page 4, lines 1-5, and all of page 5).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Maligeorgos et al. based on the teachings of Koch et al. so that fewer pins are used, power consumption is reduced, and simplicity is maintained (also EMI is reduced by using clock lines with low-swing signals)(Koch et al. page 5).

With respect to claim 87, see above rejection of claim 86.

With respect to claim 88, Maligeorgos et. al., disclose: wherein the I and Q digital signals are coupled from the fist integrated circuit to the second integrated circuit using low voltage differential coupling (see column 23, lines 45-55, use of low voltage swing differential signals).

6. Claims 89, 91-92, are rejected under 35 U.S.C. 103(a) as being unpatentable over Maligeorgos et al., (7,221,921), Koch et al. WO 03/050941 (published on 6/19/03).and further in view of Khlat et al., (U.S. 2004/0038652).

With respect to claim 89, neither Maligeorgos et al., nor Koch expressly teach: wherein the sigma delta modulator is controlled by a data rate clock, the data rate clock being programmable to provide various data rates in the serial digital signal for operation in various wireless communication systems.

In the same field of endeavor, Khlat et al., disclose: wherein the sigma delta modulator is controlled by a data rate clock, the data rate clock being programmable to provide various data rates for operation in various wireless communication systems. (see Fig. 2, where the sigma-delta modulators have fs sampling frequencies, and block 199 generates the sampling frequencies for the different system modes (paragraph [0013] and see table 1 different sampling frequencies and paragraph [0022] where PLL generates the frequencies (clocks for the ADC)).

At the time of the invention, it would have been obvious to a person skilled in the art to modify the system of Maligeorgos et al. and Koch et al. based on the teachings of Khlat et al., so that sigma delta modulator is controlled by a data rate clock, the data rate clock being programmable to provide various data rates in the serial digital bit stream for various wireless communication systems and the motivation to perform such a modification is reception of signals of different standards (for example GSM clock frequency is 13MHz, see Maligeorgos et. al.

column 11, lines 50-52 and Khlat et. al., Table 1, (sampling frequency) whereas other standards require different sampling clocks see table 1 of Khlat et. al.)).

Claims 91-92 are rejected based on a rationale similar to the one used to reject claims 89 and 88 respectively.

7. Claims 90, 93, 94 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maligeorgos et al., (U.S. 7,221,921) in view of Koch et al. WO 03/050941 (published on 6/19/03), Kim (U.S. 7,035,595) and Viswanathan (U.S. 2004/0239537).

With respect to claim 90, Maligeorgos et al. as modified by Koch et al. further teach: wherein the second integrated circuit is also configured to transmit analog data for output, without a data rate clock signal, to the first integrated circuit (Fig. 8, signals TX-I, TX-Q sent from the baseband processor to the first integrated circuit, for transmission) the first integrated circuit is configured to receive the signal output of the first output of the first integrated circuit, and modulate the data for RF transmission, (see modulation (up-conversion) performed by block 466 and subsequent RF signal transmission as shown in Fig. 8) .

Neither Maligeorgos et al. nor Koch et al. expressly teach: serial digital signals; converting digital data to be transmitted into a serial digital signal using a single bit sigma delta modulator; the first integrated circuit configured to recover the digital data to be transmitted.

However, in the same field of endeavor, Kim et al., disclose: serial digital signals (used in the transmit path between baseband and RF integrated circuits, see Fig. 1, pair of data interfaces 104, 114, used to interconnect chip 200 and baseband processor 216 of Fig. 2, Fig. 2, see column 3, lines 52-59, column 5, lines 6-7); and recovery of digital signals to be transmitted (column 3, lines 55-58, function of remodulator).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Maligeorgos et al. nor Koch et al. based on the teachings of Kim et al. so that advantages relating to the use of digital circuitry are achieved on the transmit side (Maligeorgos et al., column 16, lines 17-22)

In the field of data processing Viswanathan discloses: converting digital data into a serial digital signal using a single bit sigma delta modulator (Fig. 1, function of block 18, ¶0016-0017).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify Maligeorgos et al. based on the teachings of Viswanathan as part of pre-processing audio data so that cost, complexity and size of components used to process the signal is reduced (this teaching is applicable to Maligeorgos et al., since column 65, lines 15-23, mentions transmission of audio data).

Claim 93 is rejected based on a similar rationale used to reject claim 90 above.

Claim 94 is rejected based on a rationale similar to the one used to reject claim 93.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SOPHIA VLAHOS whose telephone number is (571)272-5507. The examiner can normally be reached on MTWRF 8:30-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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9/5/2008

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